EE 435

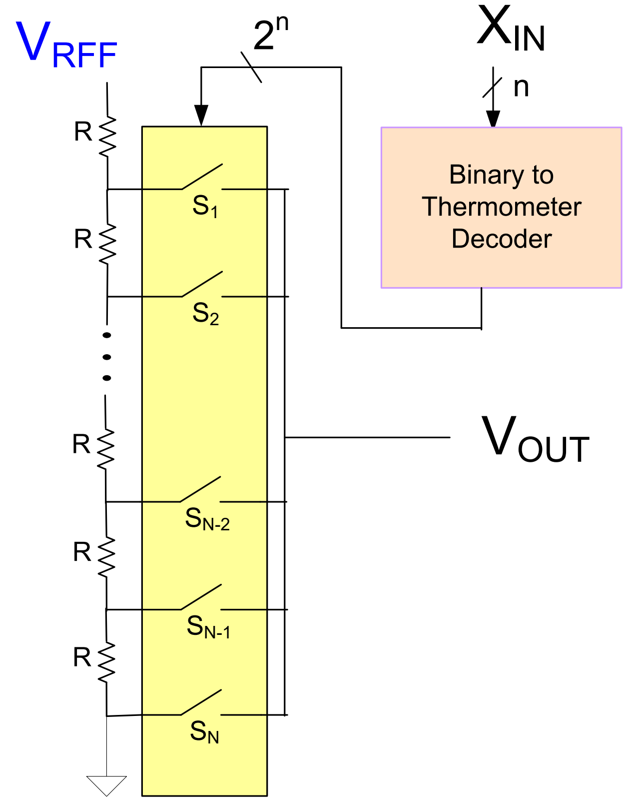
Lecture 34

Switches
Current Steering DACs

Review from Last Lecture

R-String DAC

If all components are ideal, performance of the R-string DAC is that of an ideal DAC!



Key Properties of R-String DAC

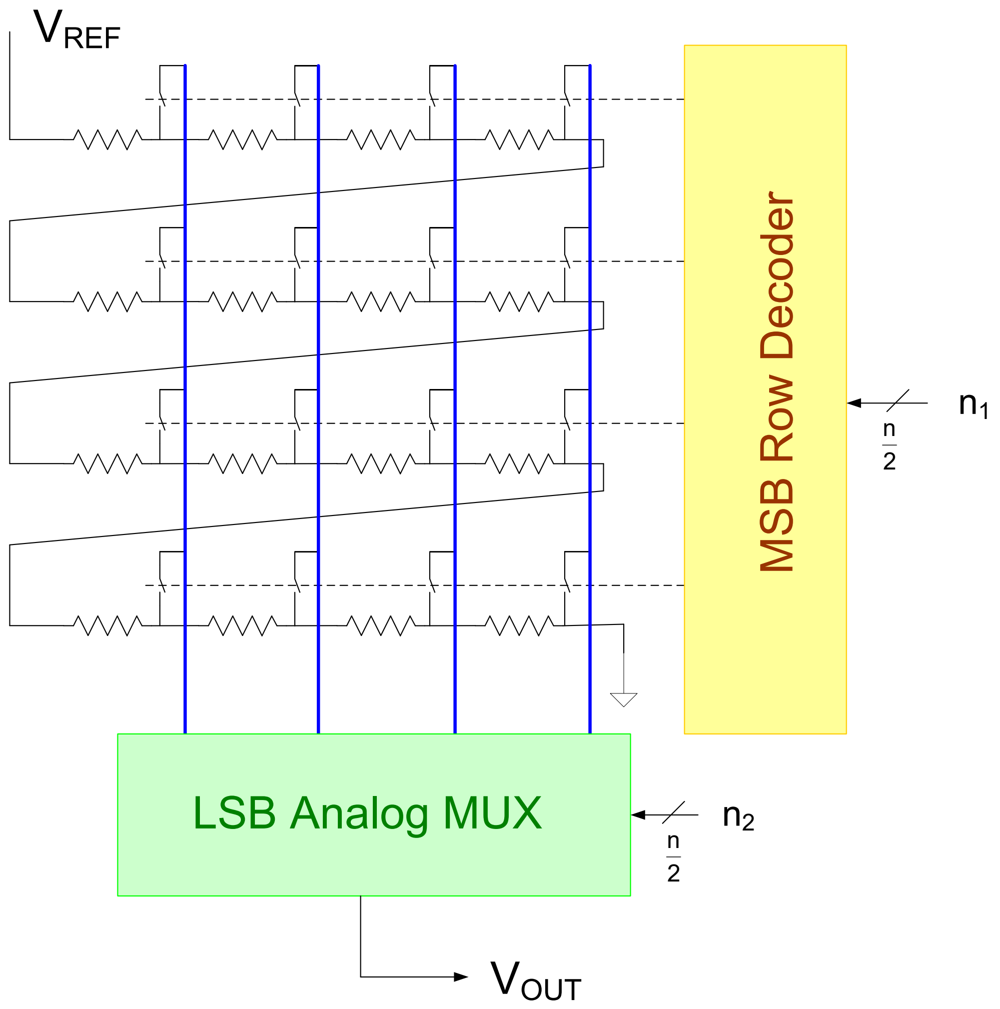
- One of the simplest DAC architectures
- R-string DAC is inherently monotone

Possible Limitations or Challenges

- Binary to Thermometer Decoder (BTTD) gets large for n large
- Logic delays in BTTD may degrade performance
- Matching of the resistors may not be perfect
  - Local random variations
  - Gradient effects
- How can switches be made ?
- Lots of capacitance on output node

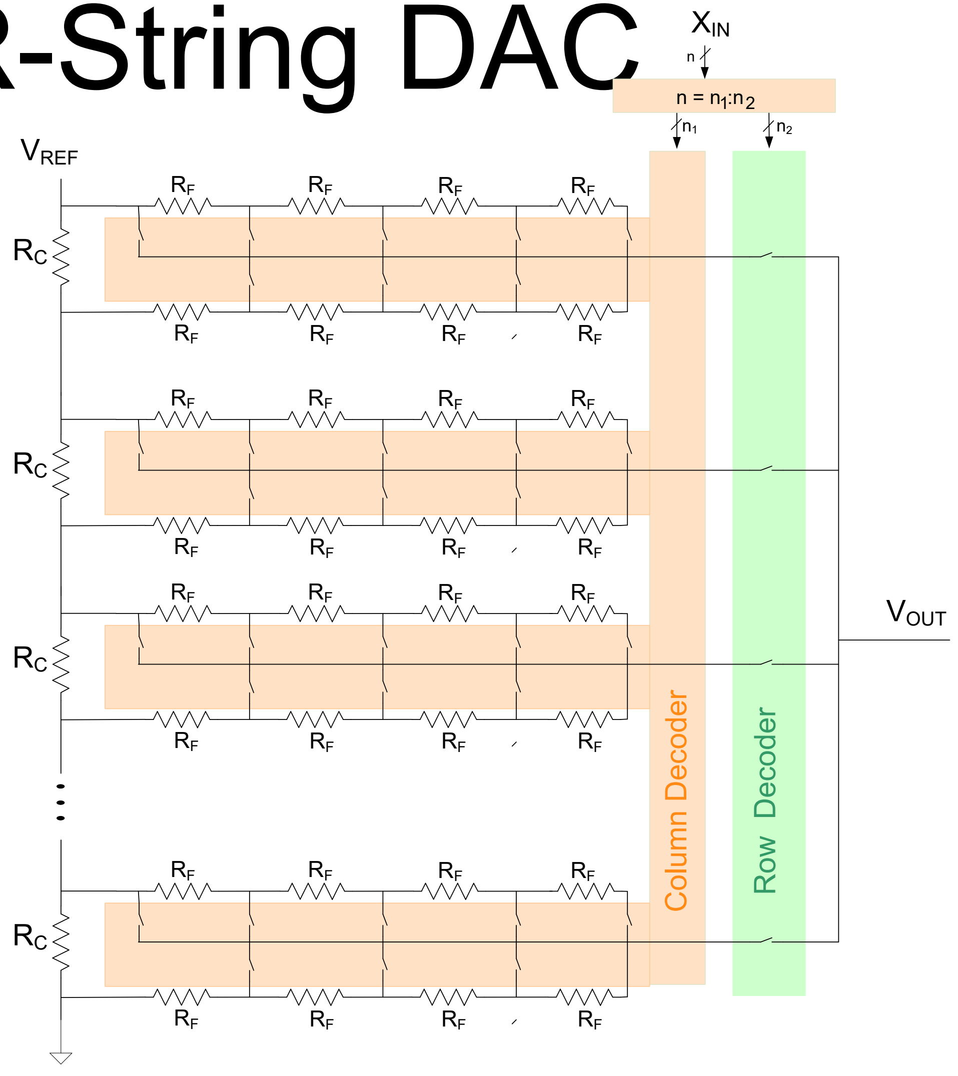
Review from Last Lecture

R-String DAC



Review from Last Lecture

R-String DAC



IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 25, NO. 6, DECEMBER 1990

A 10-b 50-MHz CMOS D/A Converter with 75-Ω Buffer

MARCEL J. M. PELGROM, MEMBER, IEEE

Note Dual Ladder is used !

A 10-b 50-MHz CMOS D/A converter with 75-Ω buffer - Get It@ISU

MJM **Pelgrom** - IEEE Journal of Solid-State Circuits, 1990 - ieeexplore.ieee.org

Abstracf -A 10-b 50-MHz digital-to-analog (D/A) converter is pre- sented which is based on a dual-ladder resistor string. This approach allows the linearity requirements to be met without the need for selection or trimming. The D/A **...**

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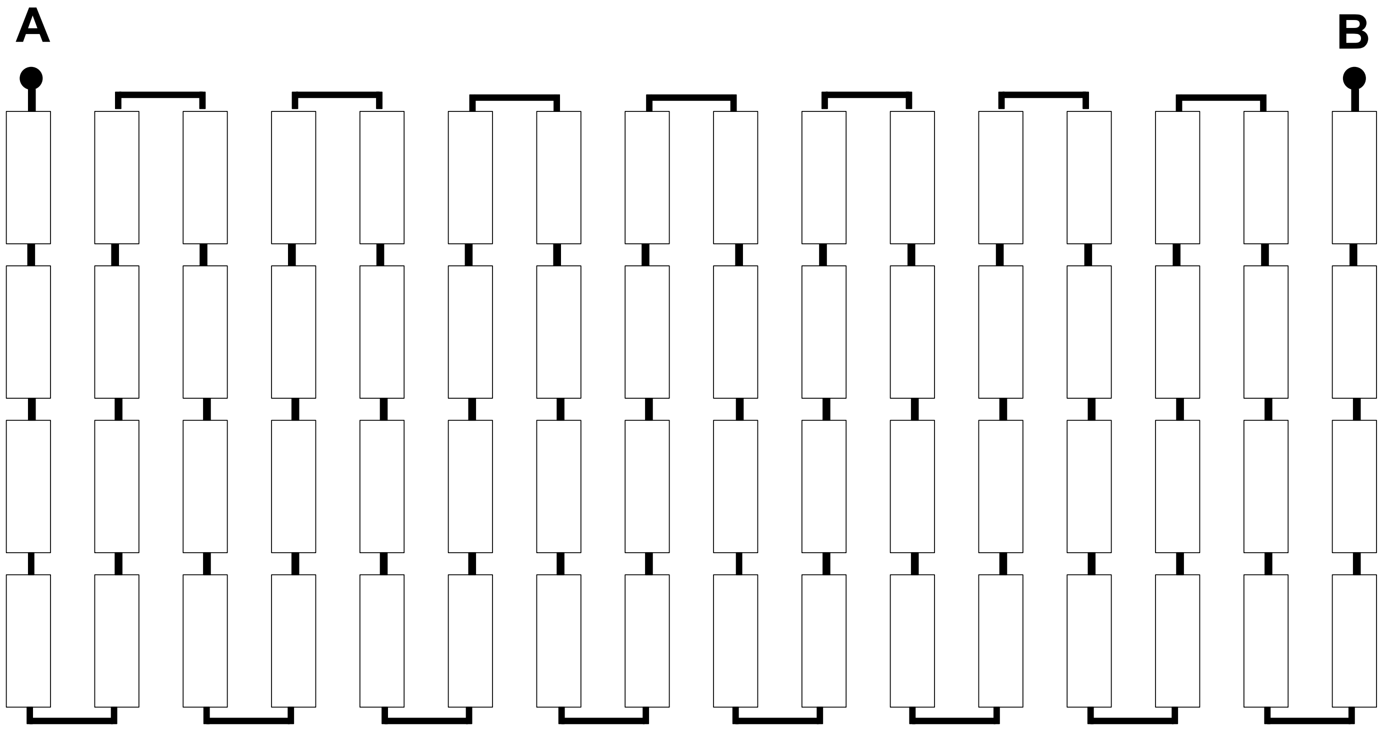
A 10-b 50-MHz CMOS D/A Converter with 75-Ω Buffer

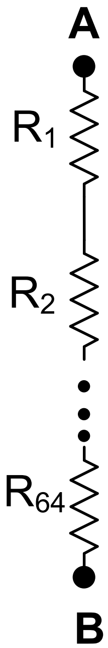
MARCEL J. M. PELGROM, MEMBER, IEEE

Abstract —A 10-b 50-MHz digital-to-analog (D/A) converter is presented which is based on a dual-ladder resistor string. This approach allows the linearity requirements to be met without the need for selection or trimming. The D/A decoding scheme reduces the glitch energy, and signal-dependent switch signals reduce high-frequency distortion. The output buffer allows driving 1 V_{pp} to 75 Ω. The chip consumes 65 mW at maximum clock frequency and a full-swing output signal. The device is processed in a standard 1.6-μm CMOS process with a single 5-V supply voltage.

Current-based circuits dump the complementary part of the signal current to ground: the power supply current is thereby twice the average signal current. If a two-sided terminated transmission line has to be fed by the high-impedance output of the current cell D/A converter, the current should be doubled to obtain the required output swing. In this case, the power supply current is four times the average signal current. A triple video D/A converter

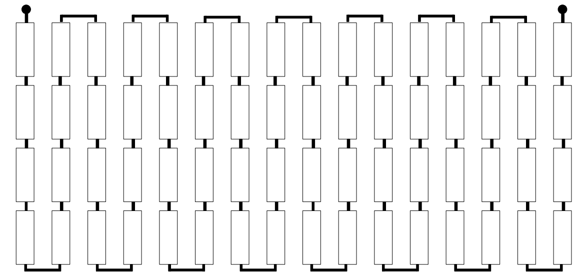
Resistor Layout

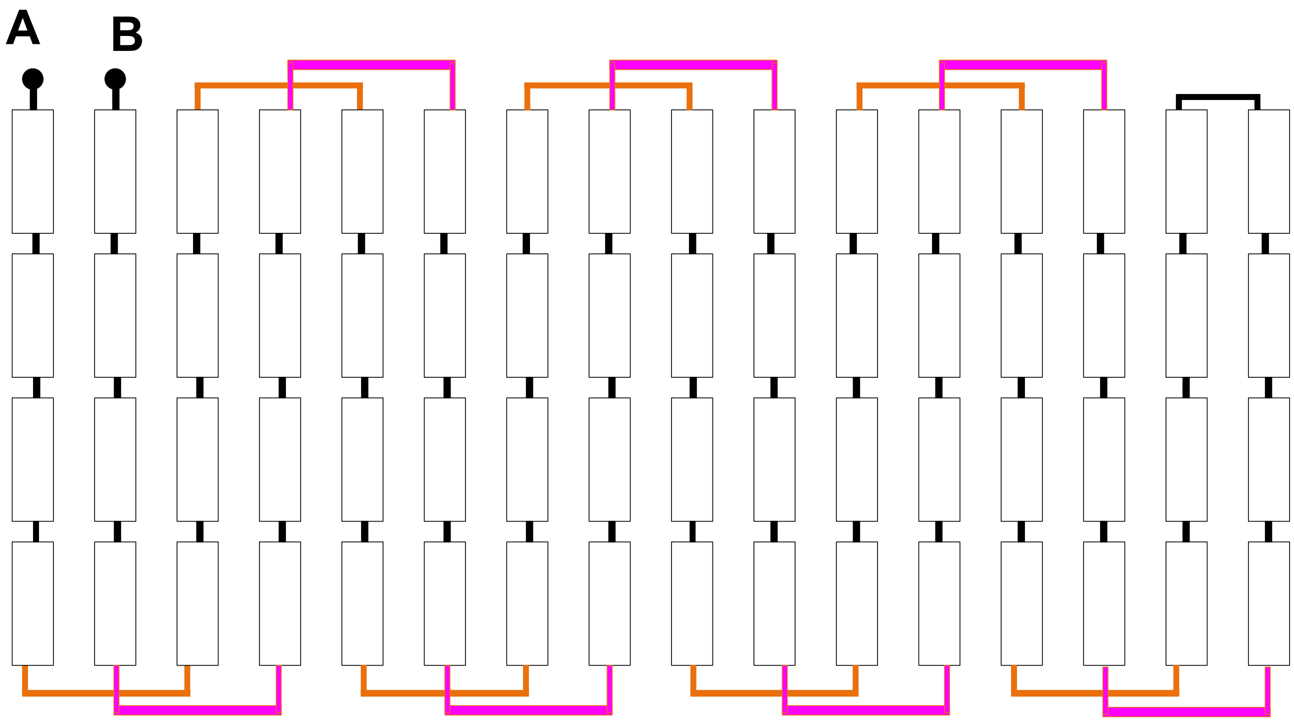


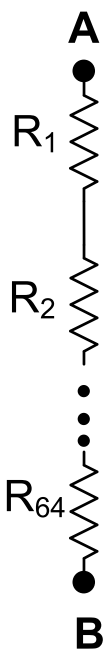


Standard Series Layout of 64 resistors

Resistor Layout

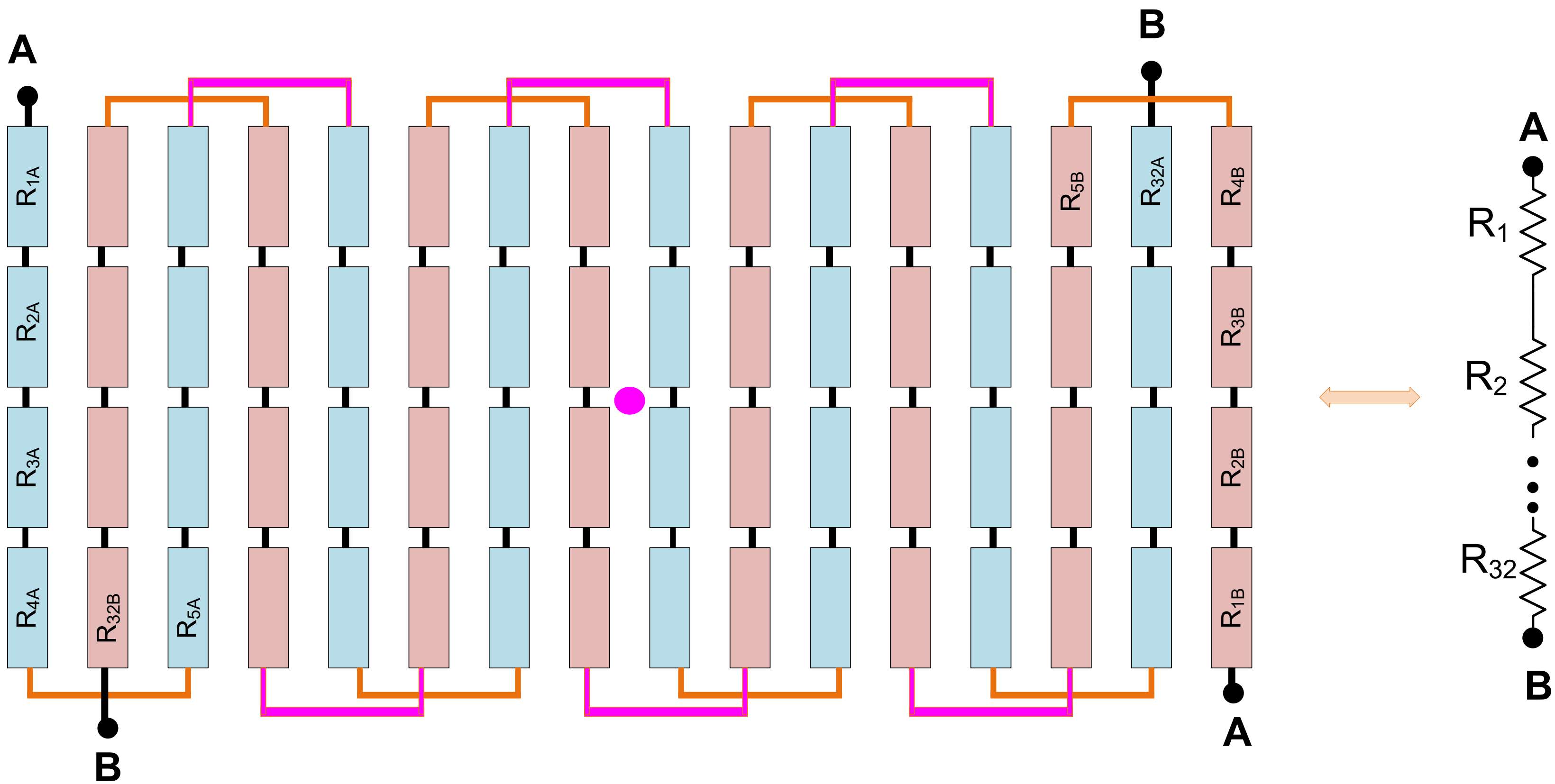






Layout of 64 resistors with reduced gradient sensitivity

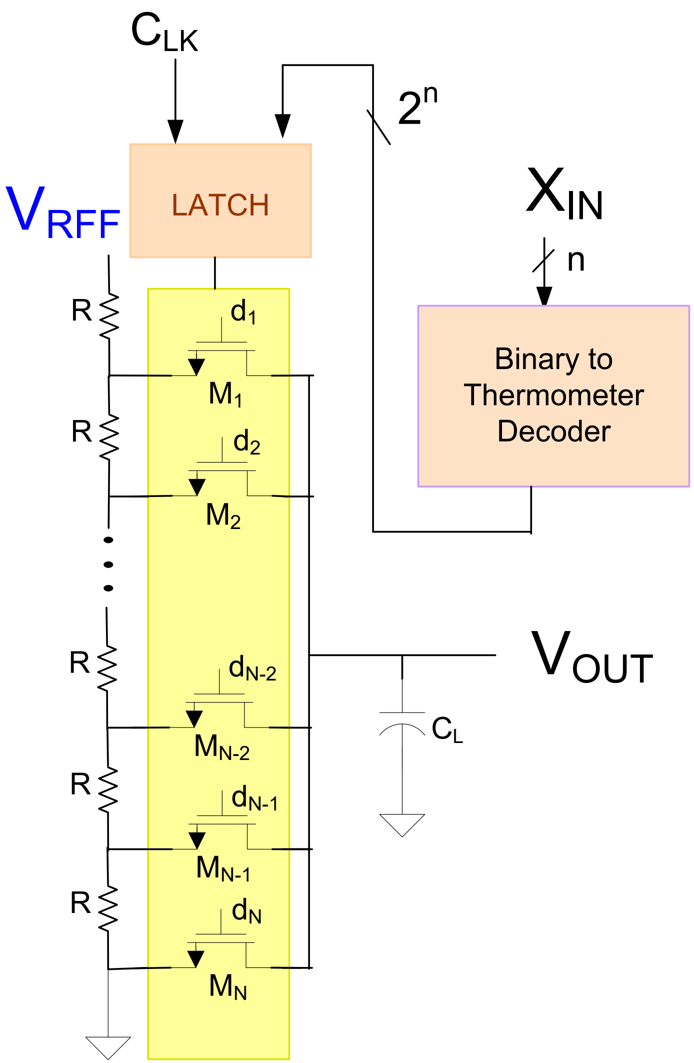
Resistor Layout

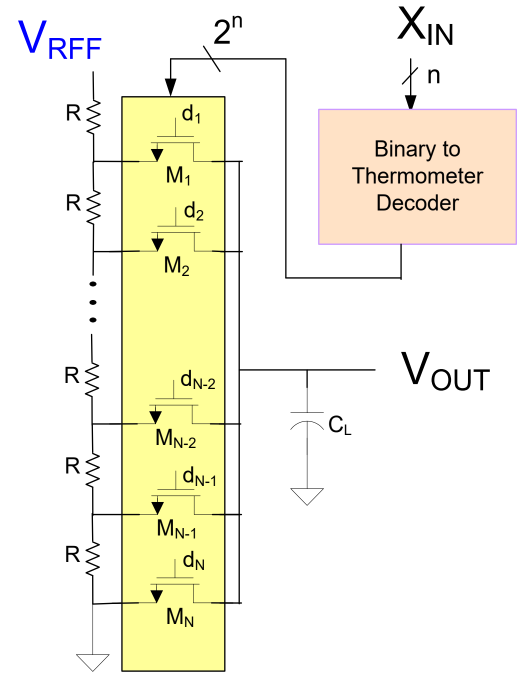


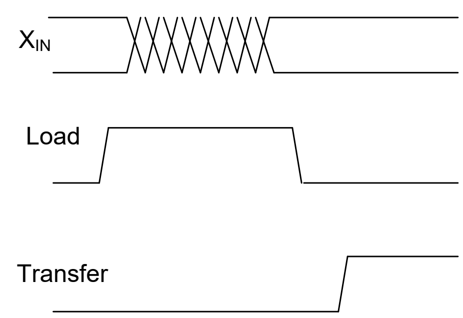
Antiparallel Layout of 32 resistors with Common Centroid

(Pelgrom used only 16 resistors)

Basic R-String DAC

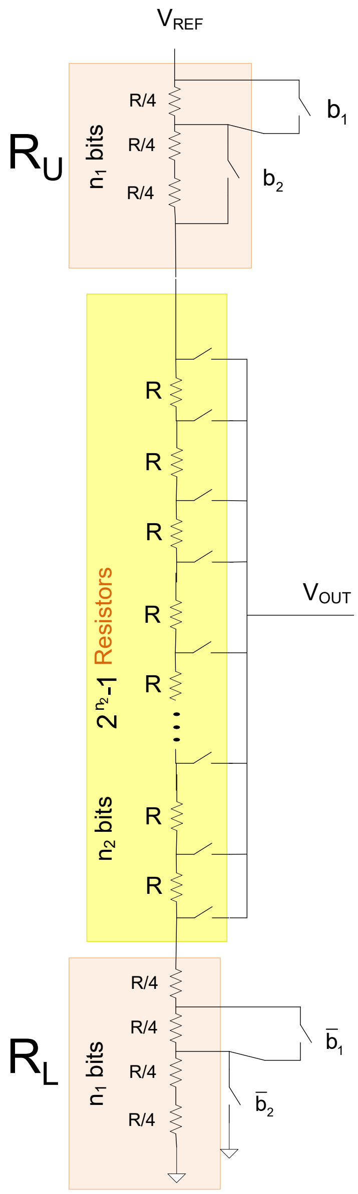






Latching Boolean Signal Can Reduce/Eliminate Logic Transients which Cause Distortion

Basic R-String DAC

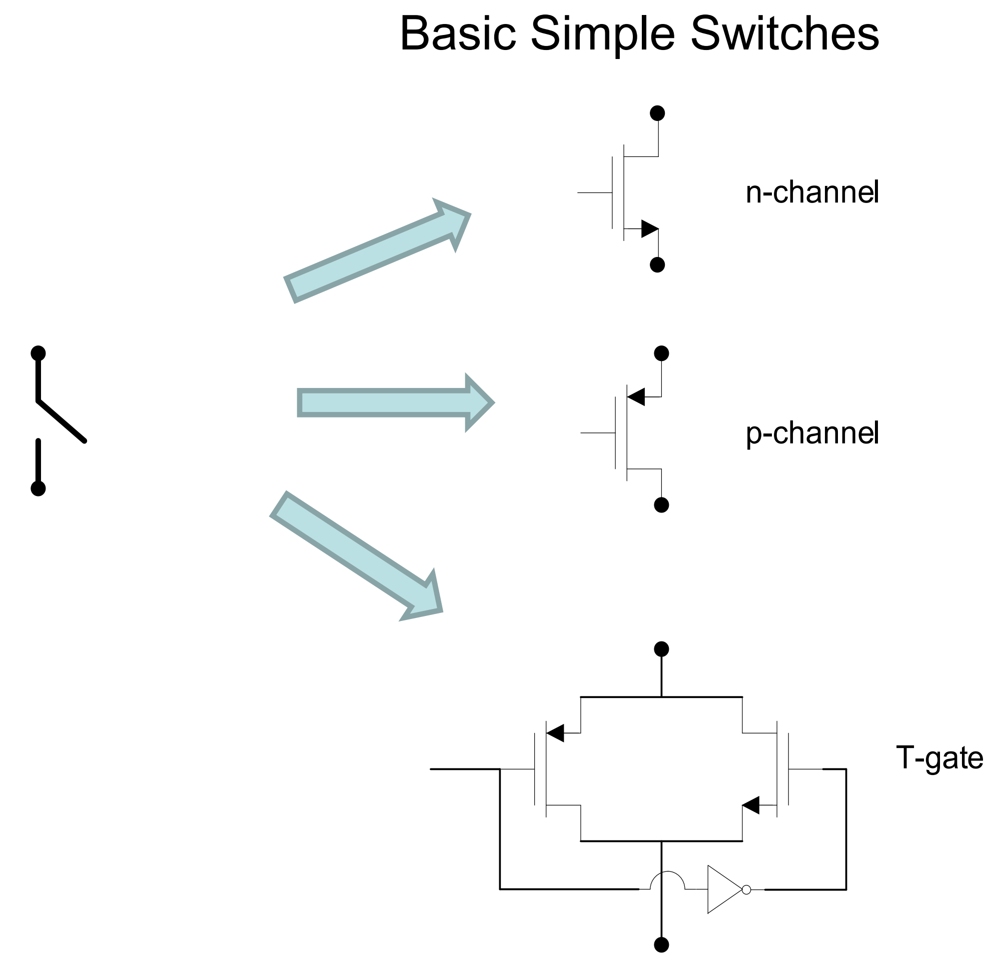


For all b_1 and b_2, $R_U+R_L=R$

- Another Segmented DAC structure
- Can be viewed as a "dither" DAC
- Often n_1 is much smaller than n_2
- Dither can be used in other applications as well

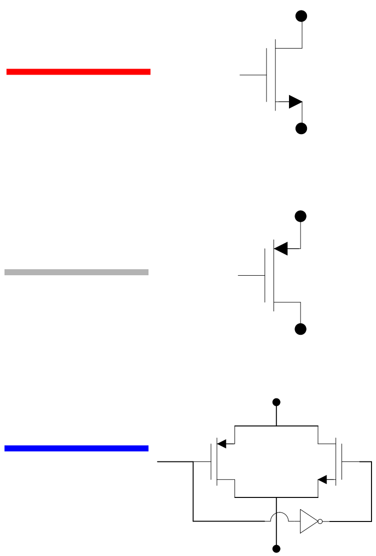
Switches used extensively in data converters !

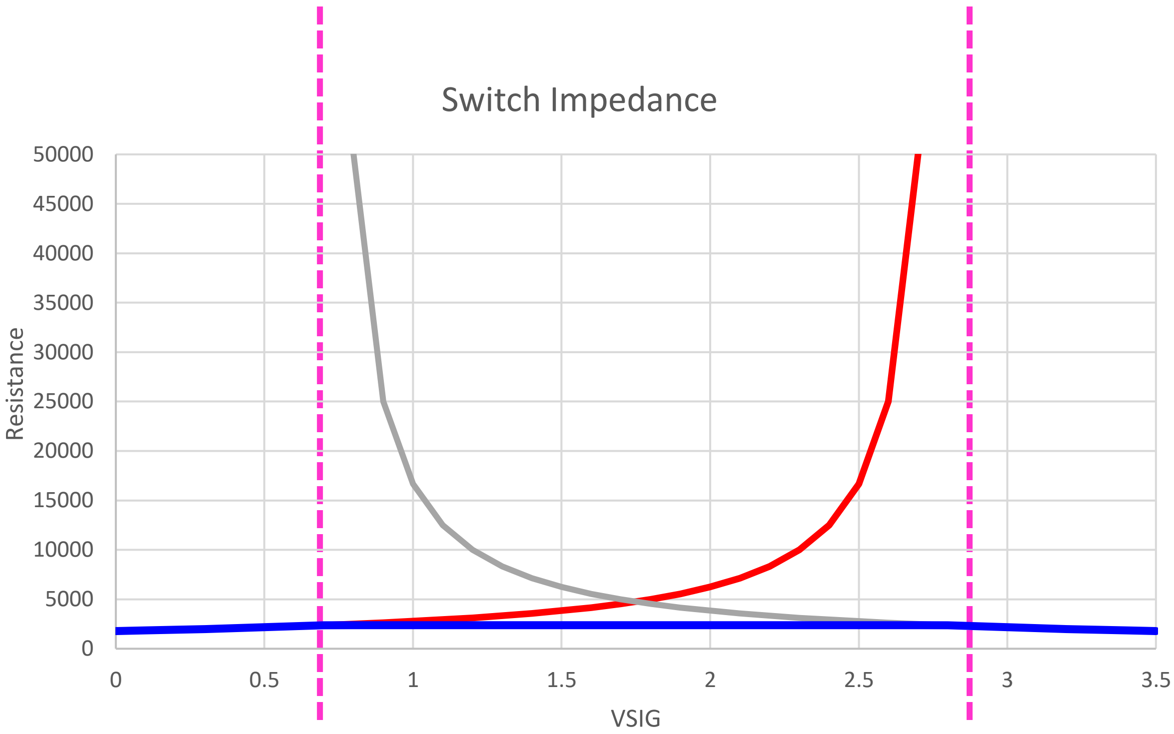
Switch Implementation Issues



Switch Implementation Issues

V_{THn}=0.7
V_{THp}=-0.7
W_p=3W_n
L_p=L_n
V_{DD}=3.5V





V_{SIG}: Voltage on switch when ON

Switch Implementation Issues

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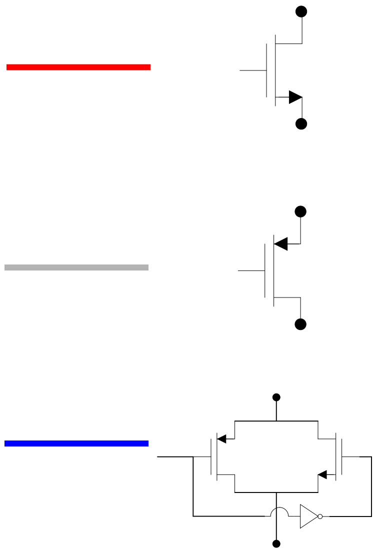

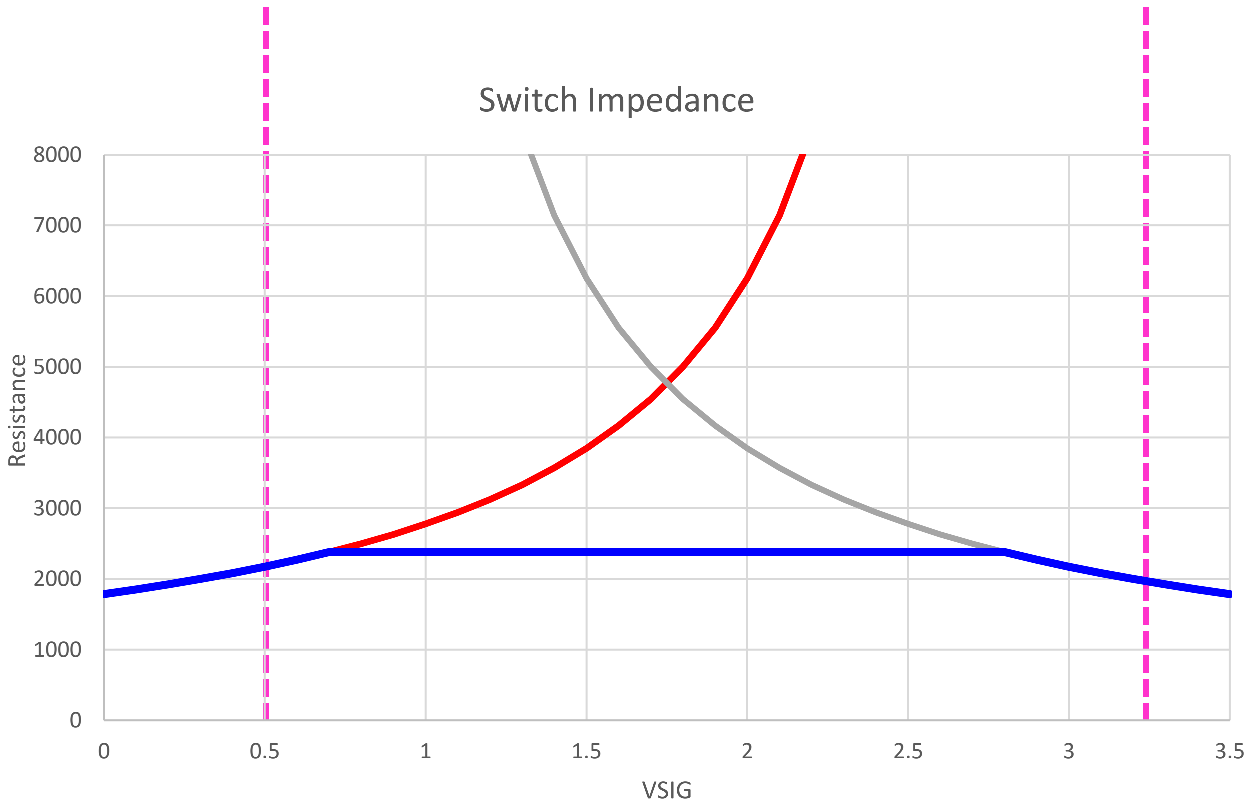

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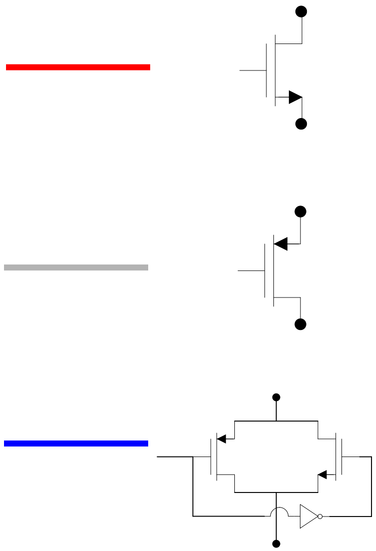
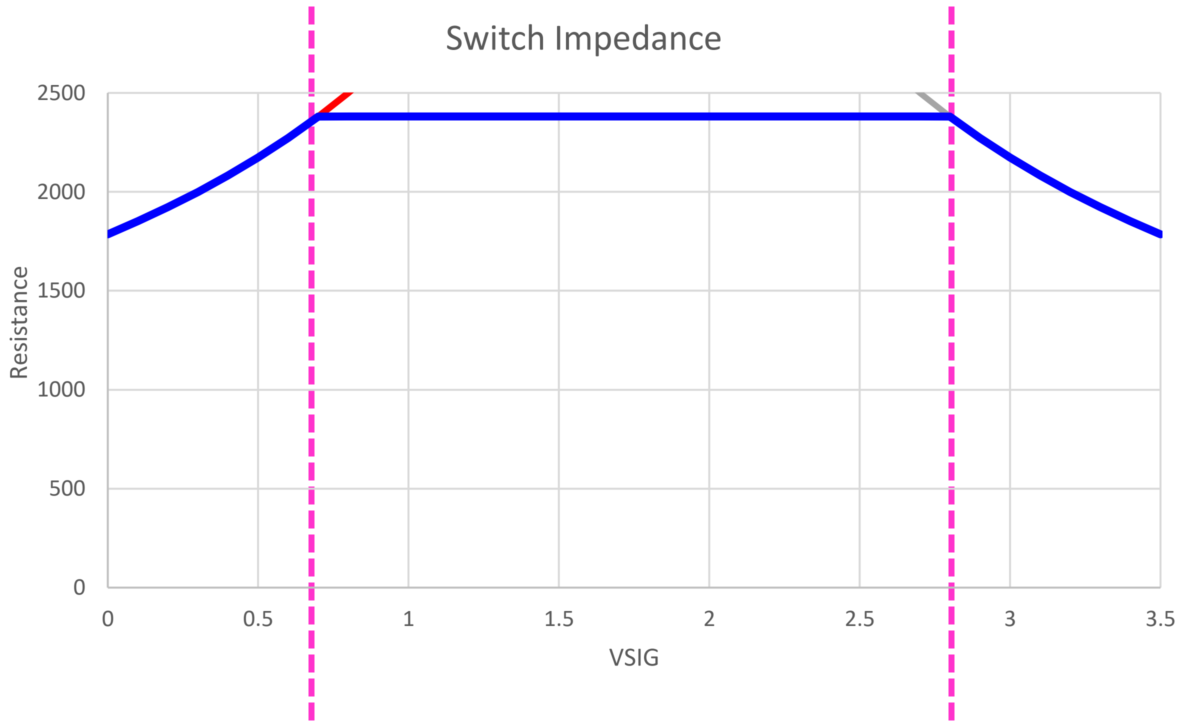


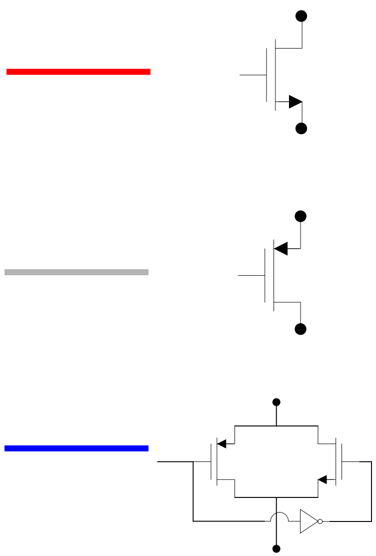


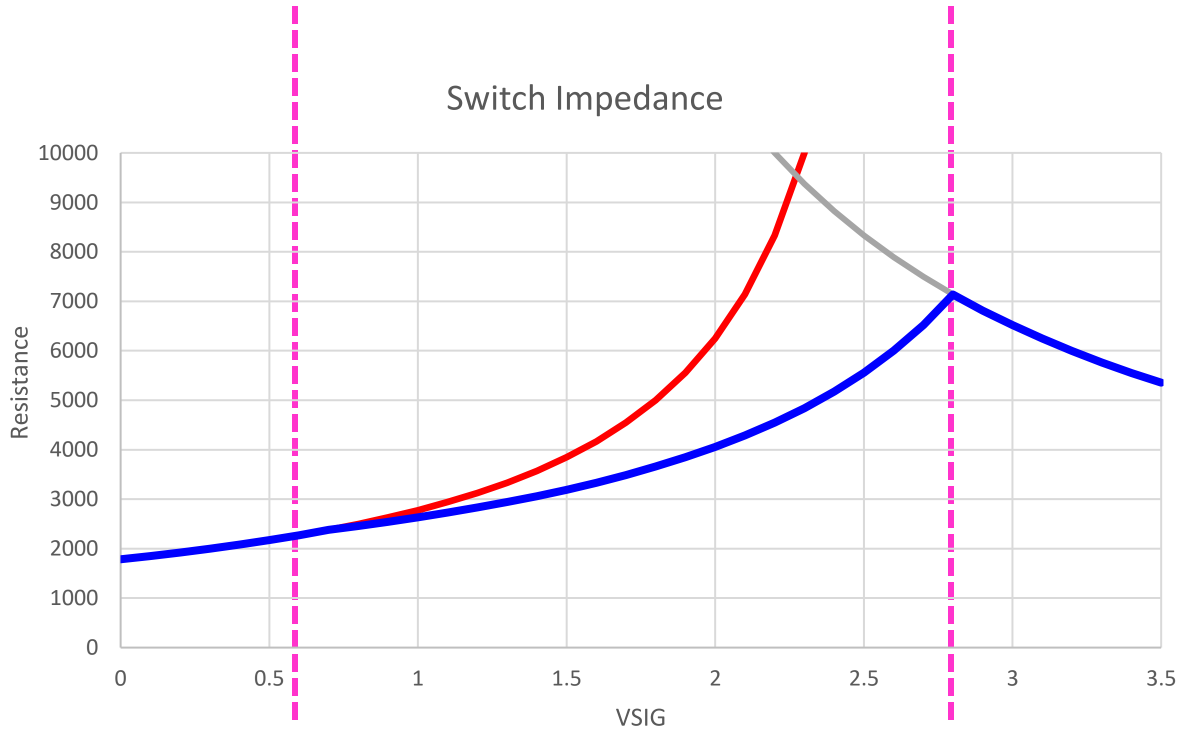
Transmission Gate Impedance Can be Reasonably constant

Switch Implementation Issues

Equal-Sized Switches

V_{THn}=0.7
V_{THp}=-0.7
W_p=W_n
L_p=L_n
V_{DD}=3.5V

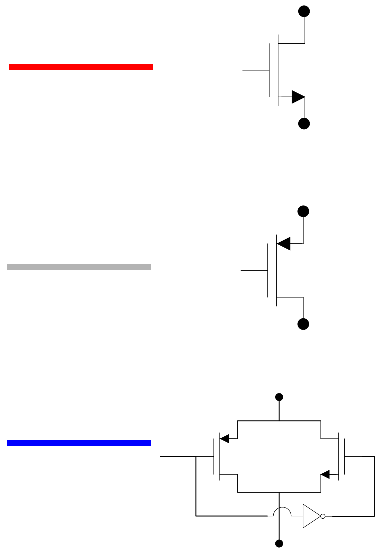


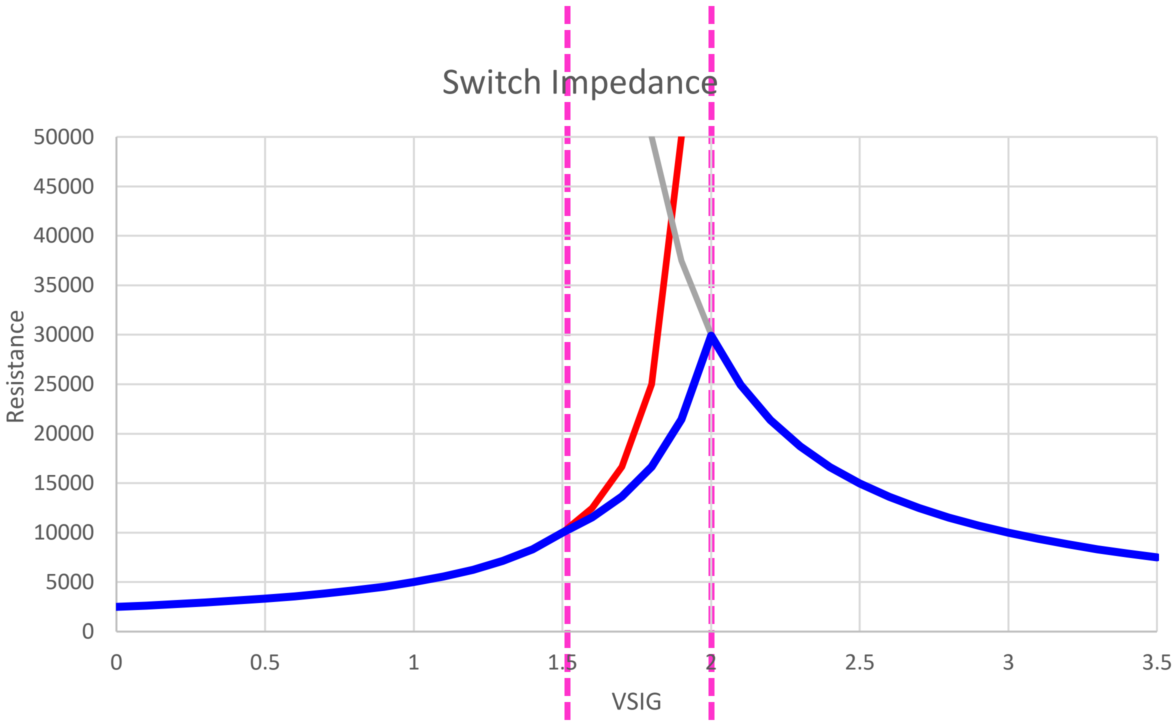


Switch Implementation Issues

Equal-Sized Switches
High Threshold Voltages

V_{THn}=1.50
V_{THp}=-1.5
W_p=W_n
L_p=L_n
V_{DD}=3.5V



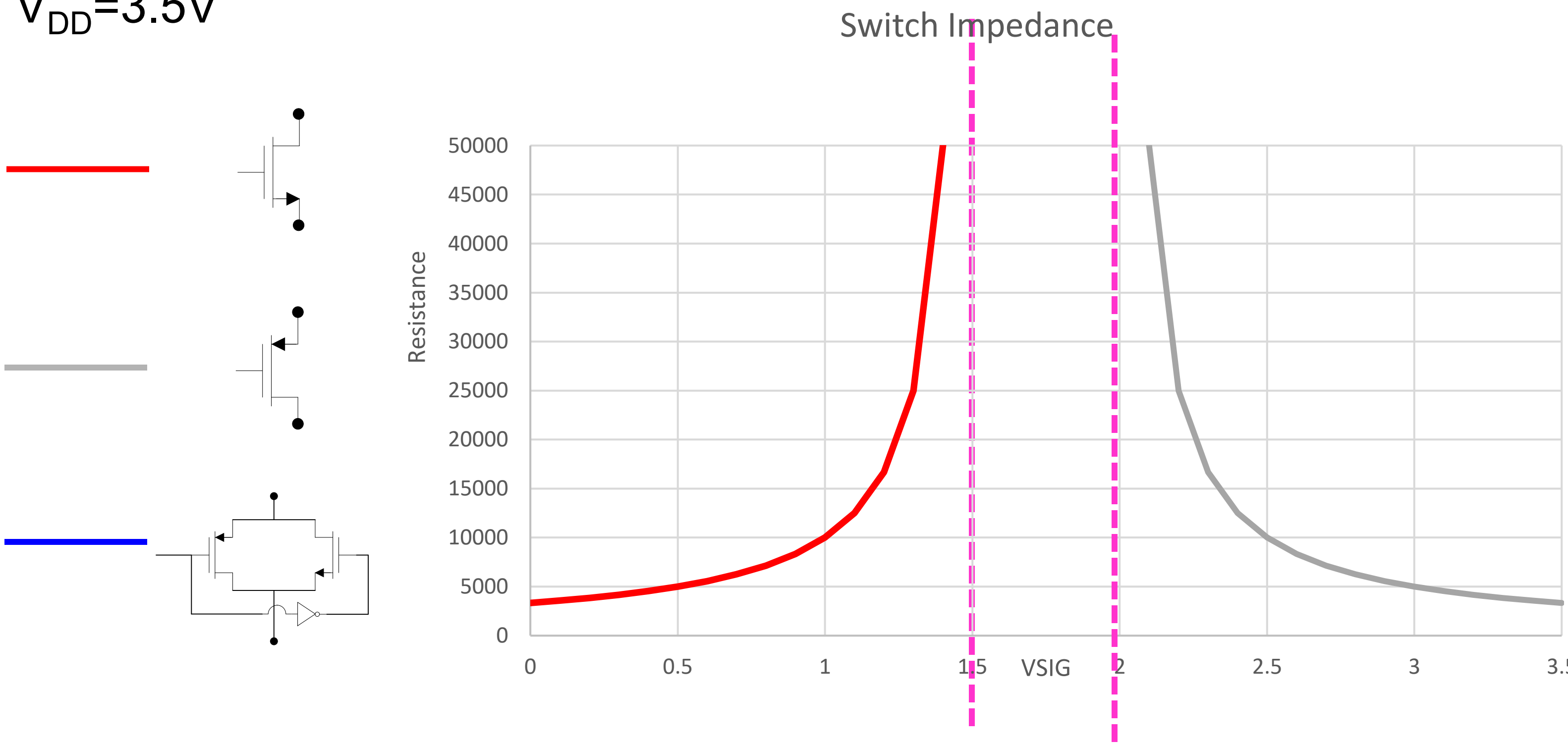


Even Transmission Gate Does Not Perform Well

Switch Implementation Issues

V_{THn}=2.0
V_{THp}=-2.0
W_p=3W_n
L_p=L_n
V_{DD}=3.5V

Tough unlikely, this is what would happen if very high threshold devices were used



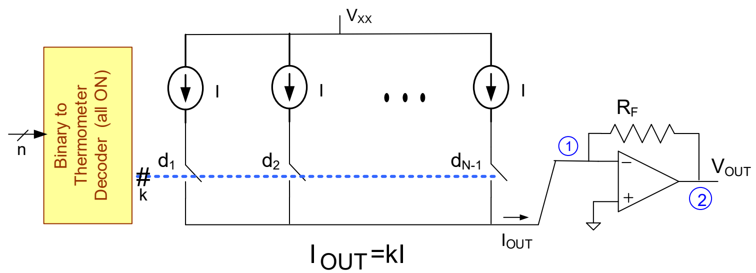
Gap where neither switch is working

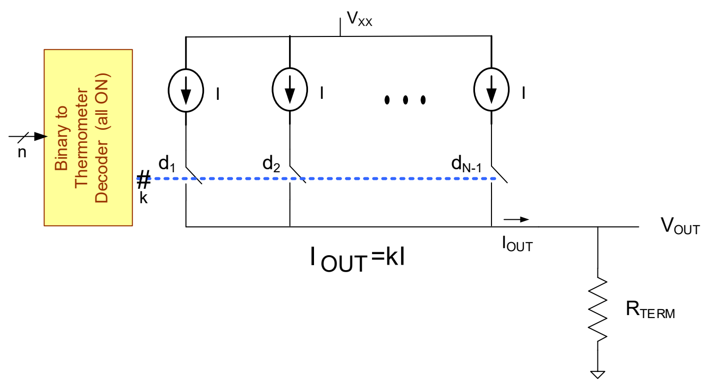
Current Steering DACs

Current will be "steered" to a resistive load (on chip)

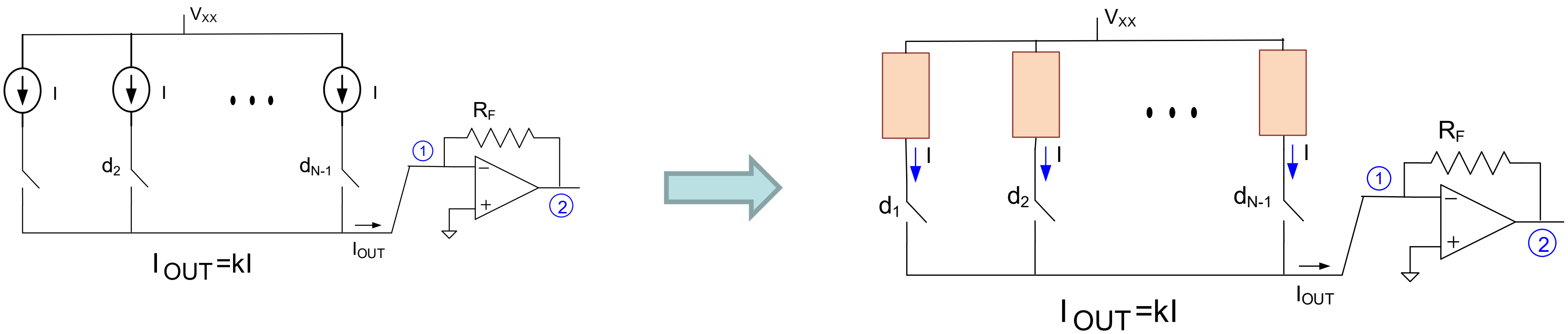
Output could be a current (user supplies load)

Basic Concept of Current Steering DACs

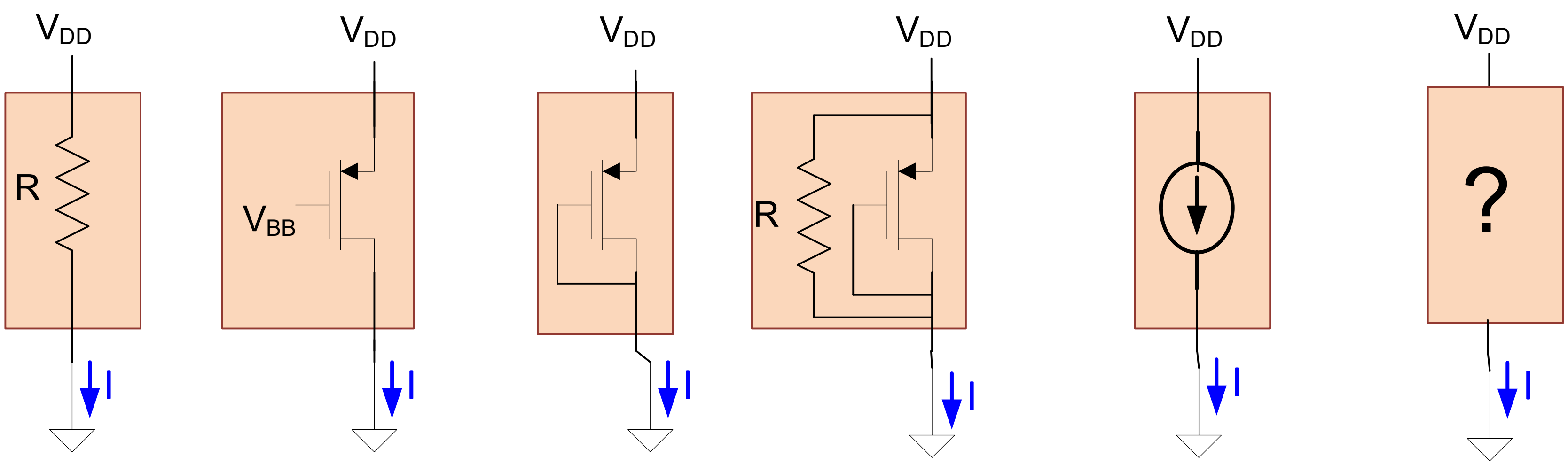




Current Steering DACs

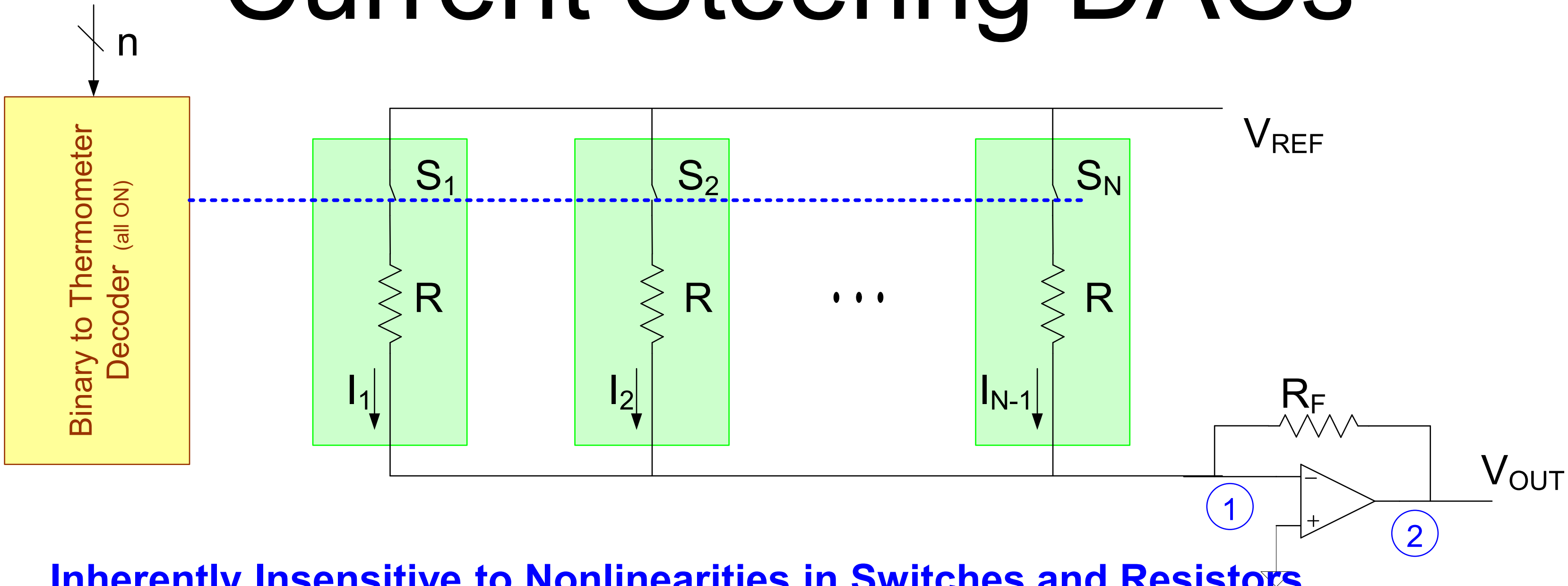


What is important is the current generated, not whether it comes from a “current source”



Many potential current generator blocks, just require that all be ideally identical

Current Steering DACs



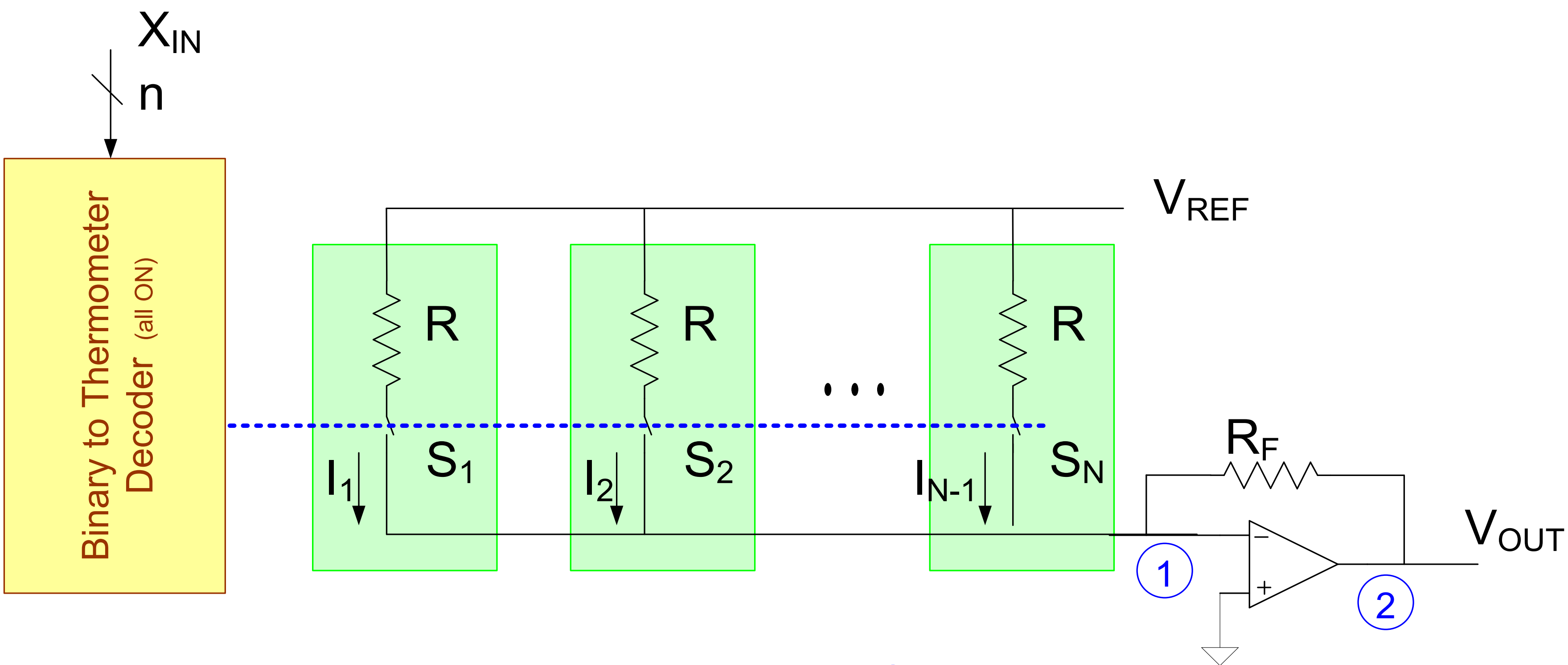
Inherently Insensitive to Nonlinearities in Switches and Resistors

- Termed "top plate switching"
- Thermometer coding
- Excellent DNL properties
- INL may be poor, typically near mid range
- INL is a random variable with variance approximately proportional to area
- Area gets large for good yield with large n

$$\sigma = \frac{A_{PEL}}{\sqrt{A}}$$

- Each additional bit of resolution requires a factor of 2 increase in area if same sized resistors are used
- Each additional bit of resolution requires another factor of 4 increase in area to maintain the same yield

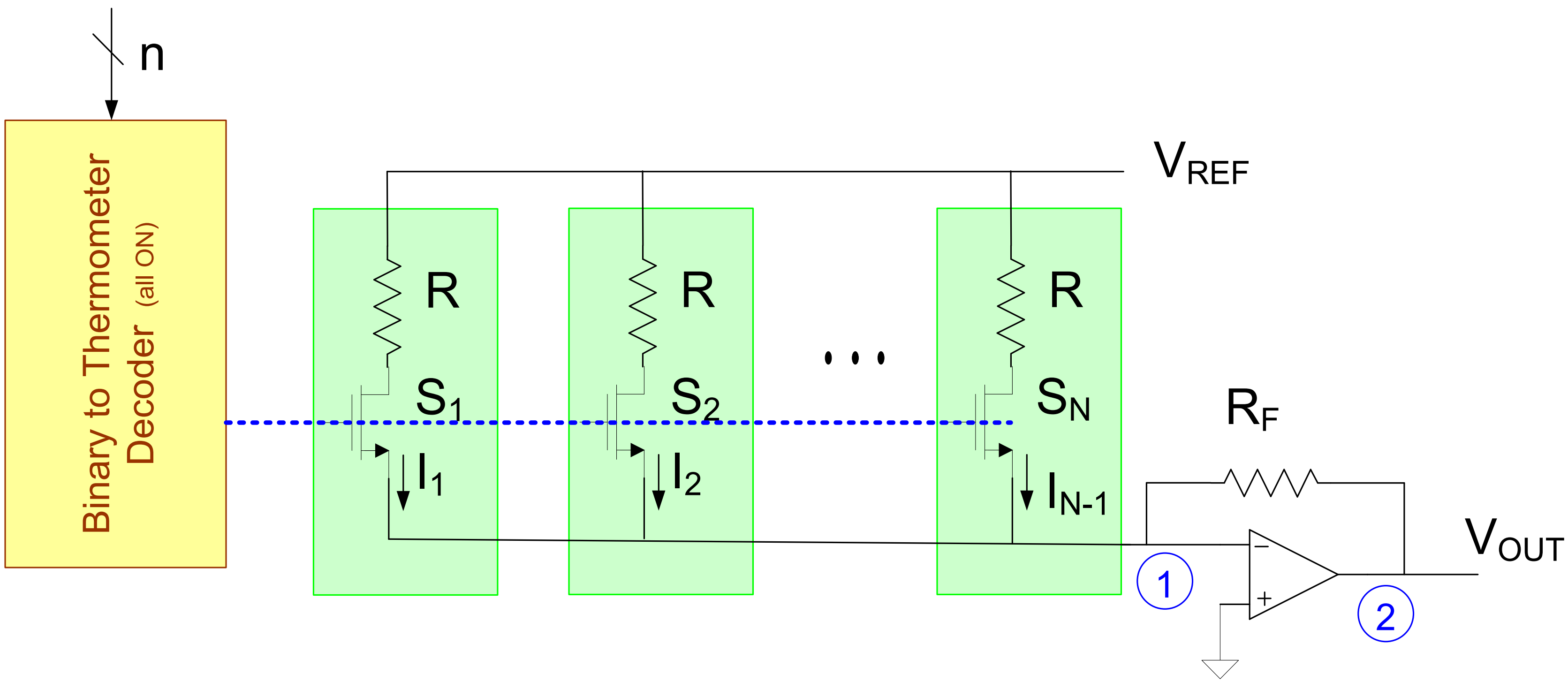
Current Steering DACs



Inherently Insensitive to Nonlinearities in Switches and Resistors
Smaller ON resistance and less phase-shift from clock edges

- Termed “bottom plate switching”
- Thermometer coded

Current Steering DACs



Transistor Implementation of Switches

Stay Safe and Stay Healthy !

End of Lecture 34